Layout Controlled One-Step Dry Etch and Release of MEMS Using Deep RIE on SOI Wafer

Liu Haobing and Franck Chollet

Abstract—**Deep reactive ion etching (DRIE) of silicon on insulator (SOI) wafer has become a popular method to build microelectromechanical systems (MEMS) because it is versatile and simple. However when the devices using this technology become large in size or have compliant beams, the stiction occurring during the HF wet release is a serious problem. We have observed that some structure patterns could be wet released more easily than others. In this paper, we discuss the relationship between structure patterns and their stiction property, and describe the notching effect, which is found to be the mechanism behind this dependence. We finally provide simple mask layout design rules to utilize this effect to our advantage. These rules allow etching the structure and releasing it with the same DRIE step, without any wet process. Alternatively, this method will completely remove the stiction appearing during wet release or other further wet processes. We show the application of these rules on the fabrication of a large moving stage. [1636]**

Index Terms—**Deep reactive ion etching (DRIE), microelectromechanical systems (MEMS), notching, release, silicon on insulator (SOI), stiction.**

I. Introduction

DEEP REACTIVE ion etching (DRIE) of silicon on insulator (SOI) technology is usually considered one of the easiest way to build high aspect ratio MEMS devices. Its usefulness has been clearly established by commercial products and MEMS researchers which have used it [1]–[4]. With only one mask, high aspect ratio structure can be formed by DRIE. After wet etching of the oxide layer in an HF solution, the device structures are released and can move freely. This process works well when the structure is simple, small, and very stiff in the vertical direction. However, MEMS devices built on SOI wafer are becoming more and more complicated and large (e.g., several millimeters). For such devices, stiction problem during release is still a concern. Stiction happens when the wafer dries and microstructures are pulled to the substrate by surface tension or capillary forces at the receding rinse liquid/air interface [5]. Then a combination of forces appearing between the structure and substrate, e.g., van der Waals forces and hydrogen bonding, keeps them firmly bonded to each other. The adhesion force is so strong that a force large enough to detach them usually destroys the microstructure [6].

Many efforts have been used to reduce the stiction and increase the release yield [7]. Mechanical approaches include creating bumps on the underside of the structure layer [8], temporarily stiffening the microstructure with polysilicon links [9], or building polymer supporting columns that can be dry etched after the wet release [10]. Other physical approaches include avoiding wet process by using HF vapor [11], reducing surface tension by replacing water with methanol before drying, using hydrophobic coating layer [12], avoiding liquid drying process by freeze-drying or supercritical drying [13], or using charge controlled overetching [14].

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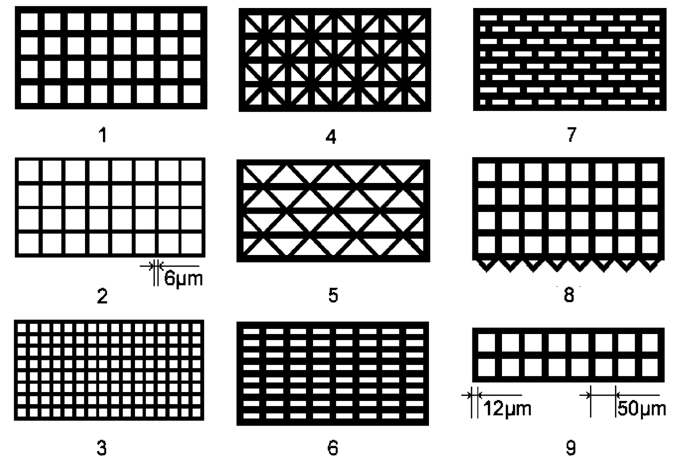

Fig. 1. Patterns for release test on 50 μm thick SOI wafer.

Although some of the existing approaches have reported high microstructure release yield, they often need complicated process or facility (e.g., CO_2 supercritical drying), and the easier methods do not achieve good results [7]. In this paper, we will introduce a method that is simple but effective for releasing microstructures built on SOI wafers.

II. Mesh Patterns and Their Release Properties

During the fabrication of actuators with the DRIE process, we observed that some mesh patterns seldom experience stiction while others almost always did. We investigated this phenomenon thoroughly by using mesh with different line width, pattern size and pattern shape at the end of an array of cantilever of different length. Fig. 1 shows the nine mesh patterns used for the test. Pattern 1 has a square unit with 12 μm line width and 50 μm gap. Pattern 2 changes the beam width to 6 μm, and pattern 3 changes the gap to 25 μm. Patterns 4 to pattern 7 adopt different shapes. Pattern 8 adds some so called anti-stiction tips on one side, and pattern 9 reduces the area to half of pattern 1.

We then noted the maximum beam length that get released after a standard etch and wet release process (Fig. 2). The results are shown in Table I.

The result shows a clear contrast. Patterns 1, 2, 8, and 9 easily stick to the substrate, as beams as short as 200 μm can not surely

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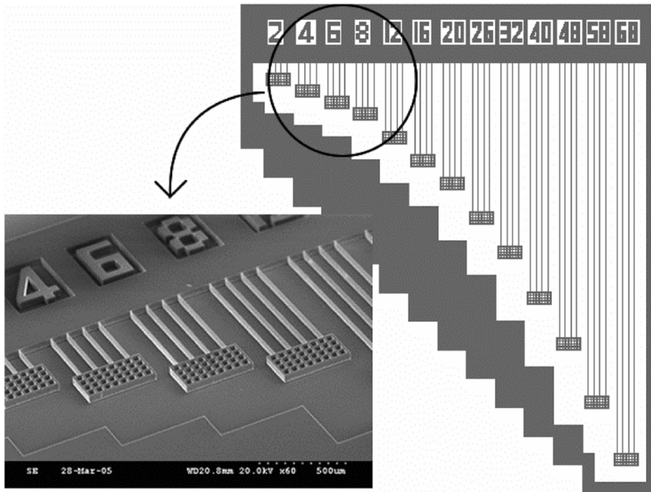


Fig. 2. Release test chip layout and SEM view.

TABLE I
RESULT OF THE PATTERN RELEASE TEST

Pattern	Maximum released beam length (μm)		
	Sample1	Sample2	Sample3
1	800	200	200
2	1200	400	200
3	6800	6800	6800
4	6800	6800	6800
5	6800	6800	6800
6	5800	6800	5800
7	5800	5800	6800
8	400	200	200
9	200	200	400

resist the stiction. On the other hand, patterns 3–7 look mostly invulnerable to stiction.

By analyzing closely the result we found that there are three factors influencing the release outcome: The mesh density or pattern gap, the pattern shape, and the mesh beams width.

III. Notching Effect With Deep RIE on SOI Wafer

After investigating the samples in SEM, we found that a pattern-dependent notching effect [15]–[17] is the mechanism for the phenomenon. Fig. 3 compares the cross-sections of patterns 1 and 4 after deep RIE and before the wet release.

The lower surface of pattern 1 remains flat, and vulnerable to capillary forces that pull the structure down and stick it to the substrate. In contrast, the lower surface of pattern 4 is rough and has micro bumps which effectively inhibit the stiction mechanism during wet release. These bumps are formed by a special type of under-etching called notching, typically occurring during DRIE on SOI wafers. The notching effect is the opening of a narrow horizontal groove (the "notch") in a conductive material at the interface with an underlying insulator [15], which is greatly related to the trench aspect ratio and shape of the pattern.

Notching effect has been observed and usually considered as a kind of charging damage during the plasma etching process of IC fabrication on SOI wafers [17]. Generally, the micro charging is brought out by the directionality difference between ions and electrons in the plasma sheath at the wafer surface. Actually,

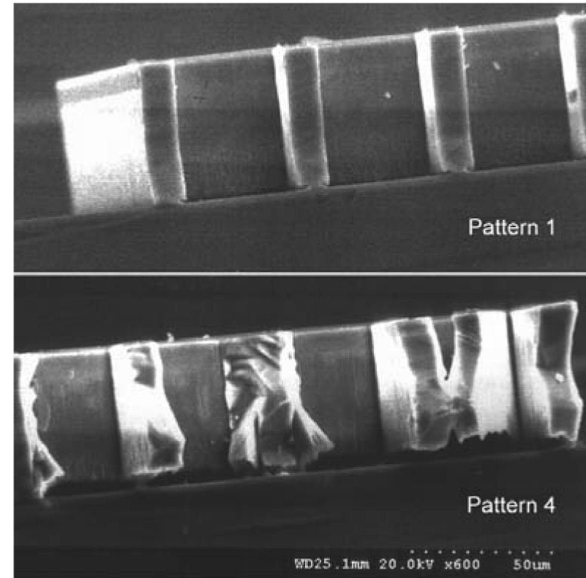


Fig. 3. Cross-section of the test structure for (top) pattern 1 and (bottom) pattern 4 showing a pattern-dependent notching under the mesh beams.

electrons have much wider angular distribution than ions, and when we etch high aspect ratio trenches, electron shadowing happens and more ions can reach the trench bottom than electrons. If there is an insulator (e.g., SiO_2) instead of conductor (e.g., doped silicon) at the trench bottom, the insulator will be charged locally, causing potential difference in the trench which deflects the injecting ions to bombard the lower corner sidewall, and initiate the notch. However, there are two major differences between the notching effect in MEMS DRIE fabrication and IC fabrication. First, a typical Bosch [18] DRIE process for MEMS differs strongly from other plasma etching process because DRIE alternates etching (SF_6 plasma) and passivation (C_4F_8 plasma) steps. Second, the SOI wafers used in MEMS have a device layer much thicker than for IC process, ranging usually between 10 and 100 μm. We try here to give an explanation of the phenomenon considering these specificities.

The DRIE process on SOI wafer is illustrated in Fig. 4. The SOI wafer is patterned by photo resist to form narrow and wide trenches. The arrows represent the direction of ions in the plasma sheath due to the DC bias and the local electrical field. As we have mentioned, Bosch process alternates etching and passivation cycles. After passivation, a thin layer of polymer covers all the trench surfaces. Then in the following etching step, the ions sputter the polymer selectively at the trench bottom due to their direction, and the unprotected silicon is chemically etched by F radicals. In summary, silicon etching happens where ions sputter away the protecting polymer.

Step **A** is the normal silicon DRIE process. The wide trenches etch quicker than the narrow ones because of the "RIE lag" [19]. In step **B**, the wide trenches have reached the oxide layer. Because of electron shadowing, the oxide areas near the side walls are charged by the more directional ions. The resulting field deflects the ions a little reducing the ions that reach this area, preventing the potential difference to go higher, and the process soon reaches a balance. The sidewalls near the wide gaps are barely attacked except by some ions reflected and scattered by

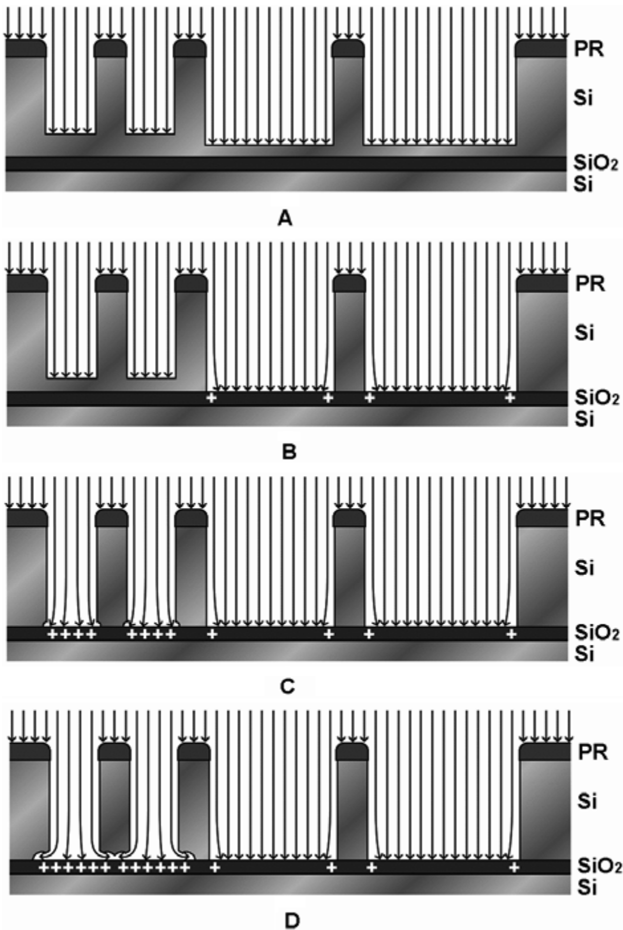


Fig. 4. DRIE of narrow and wide trenches on SOI wafer.

the exposed oxide layer. Step **C** is a few minutes later, the narrow trenches have also reached the oxide layer, and micro notches started to form. Unlike in the situation with the wide trenches, the electron shadowing is dominant in the narrow trenches, and all the bottom oxide area is charged. The injected ions are then deflected to the bottom edge of the trench, destroying the protective polymer on the lowest part of the silicon sidewall and initiating the micro notches.

Step **D** shows the growth of the notches. Once a notch has been initiated, the notched area is not protected effectively by the following passivation cycle. The oxide under the notch gets charged deflecting further the ions, and the micro notches form tunnels in a few cycles. Finally, the notch growth will slow down and stop because ions going through the notch have less and less chance to reach its end as they hit the side of the deeper notch.

The growth of the notch is shown in Fig. 5 and summarized in Fig. 6.

The trenches with different widths are fabricated on a 50 μm SOI wafer. After the wide trenches have reached the oxide layer, we continue etching the wafer for 15 min observing the cross-section of the trenches every 3 min. The curves in Fig. 6 show that once the notch is initiated, its depth increases quickly in the first few minutes of overetching, and then the growth slows down and finally stops. The final depth of notch is interestingly roughly equals to 110% of the width of the trench. This relationship exists when the trench width is below 20 μm. For wider trenches (30 μm and above), the corresponding reduction of electron shadowing is sufficient to prevent the deflection of ions and thus does not initiate the notch. The exact width where the notch starts to appear depends strongly on the trench aspect ratio but also on the thickness of the polymer layer deposited during the passivation step. This self-limiting growth dynamic is a good aspect of the notching effect, as the depth of the notch is mainly determined by the trench width (the design) instead of the overetching time (the process), making it easier to control.

The origin of the three factors influencing the release result that we mentioned in Section II can be found in the notching mechanism. Pattern density or line separation influences the trench width or aspect ratio. The mesh pattern shape also influences the trench width. Actually, triangular mesh can be viewed as having trench widths varying from 0 to a certain value and their sharp 45° angles initiate the notch more easily than the 90° corner of the square pattern because they can enhance the electron shadowing effect. For the third factor, it is obvious that thinner beams are released more easily than wider ones, especially since we know that the growth of the notch is limited.

IV. Layout Design Rules for One-Step Dry Etch and Release and Easy wet Release

From the previous analysis, in ideal situation, the structures formed on SOI wafer by DRIE can be released by notching without HF oxide etching step if the layout is properly designed. In the case that you do not want to benefit from the possibility to perform dry etch and release in one step, the layout rules will still be useful to dramatically reduce the chance of stiction during the wet release process by modifying the surface below your SOI structure.

A. For Moving Structure With Large Surface, use Triangular Mesh or Other Dense Mesh With Trench Aspect Ratio Above 2 and Proper Line Width

The triangular mesh is recommended not only because it does initiate notching more easily, but also because it is much stronger mechanically than other mesh. Pay attention to the line separation and line width. Although the notching effect also depends on the etching system and etching parameters such as passivation and etching cycle ratio, RF power, dc bias voltage, gas flow rate, chamber pressure etc, it depends mostly on the aspect ratio because its source is electron shadowing. From our experiment in a STS ICP deep RIE system with standard program, for 50 μm SOI wafer, the gap between lines should be below 25 μm to initiate notching (see Fig. 5). Another source found that for 20 μm thick SOI wafers the critical trench width to initiate nothing is 14 μm [20]. We give a trench aspect ratio of 2 as the general guide for initiating the notch, but it probably needs to be adjusted slightly according to the system used. To keep overetching time short and cater for the edge of the mesh, the line width should not be more than half the trench width.

B. Avoid Wide Trench Adjacent to Moving Structure

A wide trench is a trench with an aspect ratio below 2 according to rule A. It is often possible to cover wide trench with dummy patterns, but if some wide trenches are really needed,

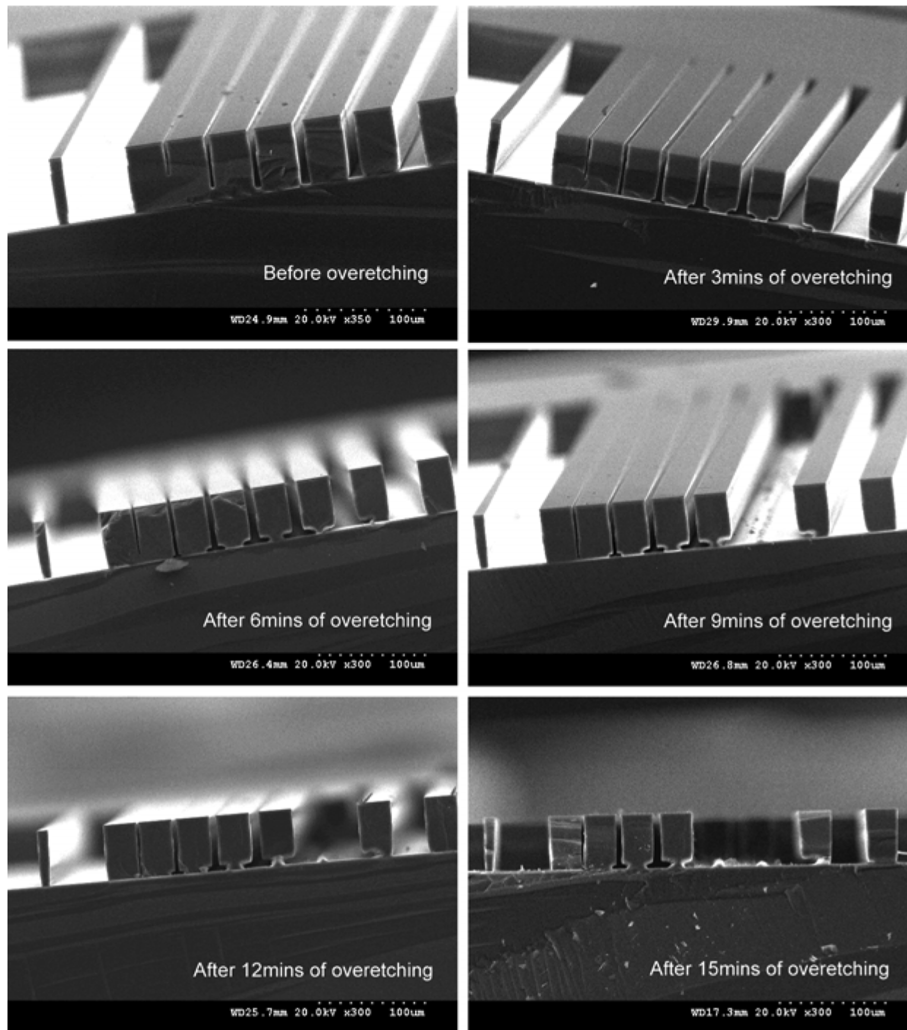


Fig. 5. Initiation and growth of notches. (Note: Some beams disappeared after 9 min because they were totally released and flew away when we cut the sample).

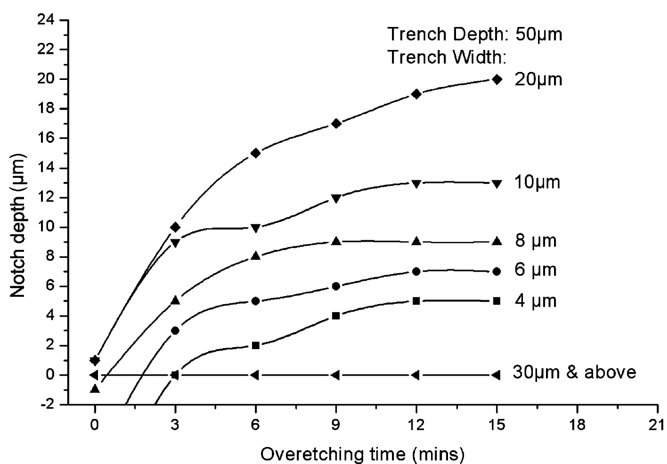


Fig. 6. Growth of the notch with time for 50-μm-deep trenches with different widths.

modify the structures between them by introducing narrow trenches or dense patterns. For example, the left of Fig. 7 shows a moving beam between two wide trenches. It can be changed to the right pattern, which has the same function and can be released by notching.

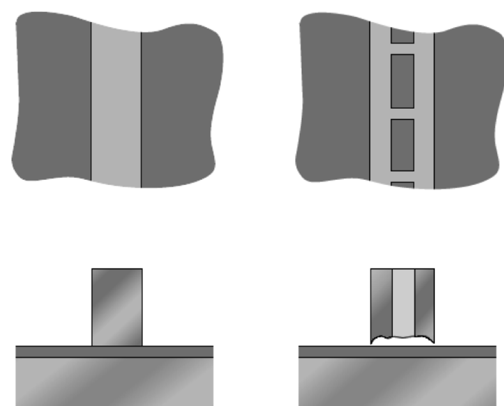


Fig. 7. Self-releasing beam (right) obtained by layout modification.

C. Avoid Wide Moving Beams

Moving beams wider than the notch that can grow under it will not be properly released. When a wide beam is needed in a structure, it can be split into two narrow beams, as the example in Fig. 7 show. From Fig. 6, we see that the widest beam that can be released will be roughly as wide as deep, providing it is surrounded on both sides by trench of proper width (here, for

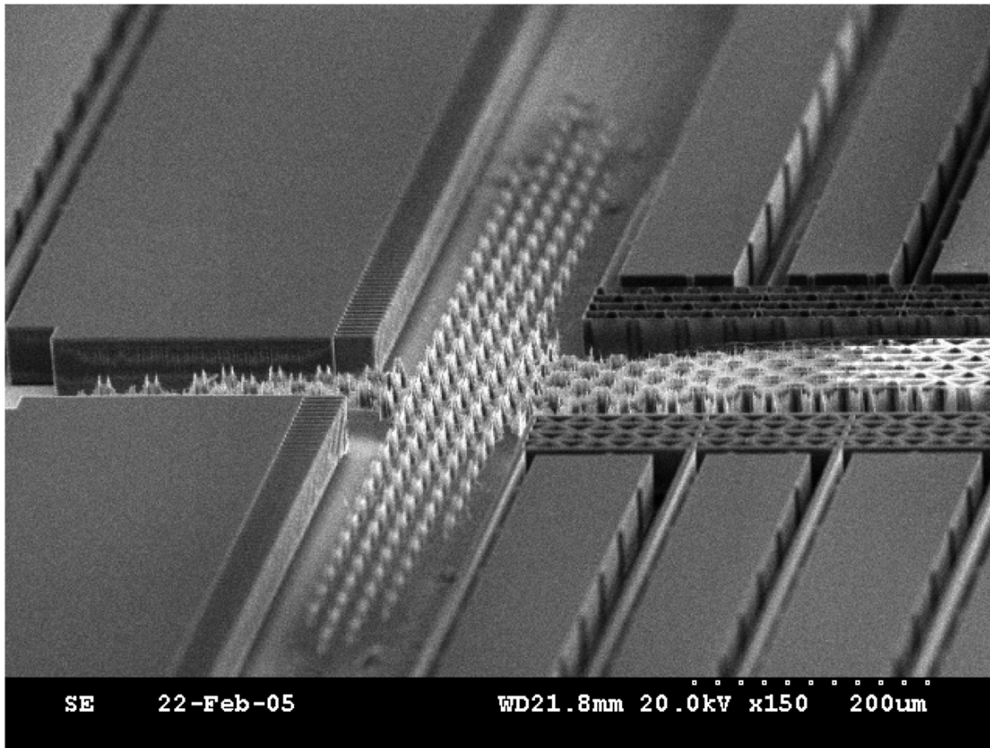


Fig. 8. Structure destroyed by overheating—the structure farther away from the anchor (located on the right) is affected first.

the 50-μm-thick device layer, it means about 50-μm-wide beam surrounded by two 25-μm-wide trenches).

D. Pay Attention to the Heat Dissipation Problem or Take Advantage of it

The back side of the SOI wafer is in contact with helium gas to cool down the whole wafer and keep it below 70°C during the etching process. Before the structure is released by notching, the heat generated on the structure surfaces is dissipated away through the underlying oxide and silicon base. However, once the thin beams have been released, this heat dissipation route is disrupted. The heat has to be dissipated to the silicon base through the anchors of the beams. If this alternative heat dissipation route is not effective enough, the released structure may overheat to above 100°C locally, burning the photoresist and causing insufficient polymer deposition, weakening the wall passivation [21], risking to destroy the structure in a few minutes (see Fig. 8). Careful design of the anchor can reduce this risk, but this method is difficult to master and may put limitations on the design. A simple way to solve the heat dissipation problem is to break-down overetching time into short etching steps and allow the structure to cool down in between. For example, if 5 min of overetching is needed, we use five 1-min etching steps, with 3 min interval in between. However, on the other hand, the heat dissipation problem can be used advantageously. A group has shown "waffle structure" [14], which consists only of patterns that are released by notching but without anchor for sinking the heat. The structure will be totally etched away in the process and can be used if necessary to open large area of empty space.

These four rules are easy to follow, and should not set any insurmountable obstacle realizing any device function.

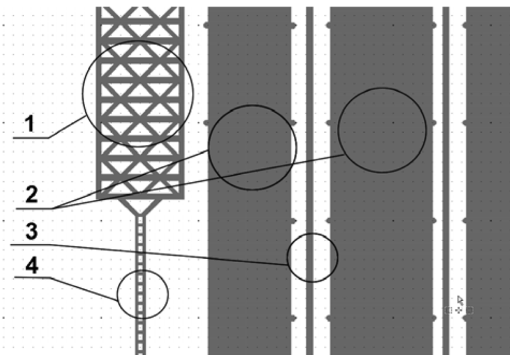


Fig. 9. Application of the rules on device layout. 1) Dense triangular pattern for moving structure. Rule A. 2) Fixed dummy patterns to cover wide gaps. Rule B. 3) Narrow moving beam obtained using narrow trenches. Rule B. 4) Isolated moving beam obtain with a split beam. Rule C.

V. Example of One Step Dry Etch and Release Process

These design rules were established during the fabrication of a switching stage [4], and they have been utilized successfully to solve the stiction problem we have met. Fig. 9 is part of the mask layout.

All the layout rules have been proved effective, and Fig. 10 shows a totally dry released structure and its bottom view. We can see that the bottom surface of the structure has been corrugated according to the mesh pattern. We have confirmed that this roughness and the increased gap below the structure effectively prohibit the stiction mechanism in a subsequent wet process.

This process allowed obtaining large devices with a large freedom of layout, as the switching device (Fig. 11) with 6 $\times$ 6-mm moving stage and using compliant suspension with 2 μm wide beams.

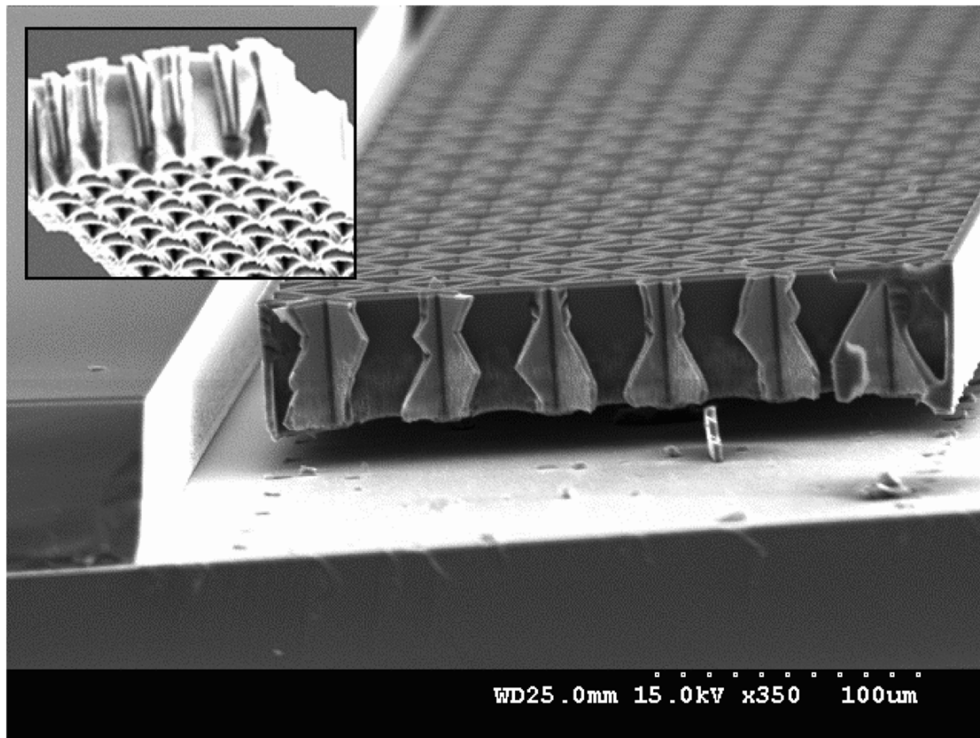


Fig. 10. Dry released patterned structure and (inset) view of the structure bottom.

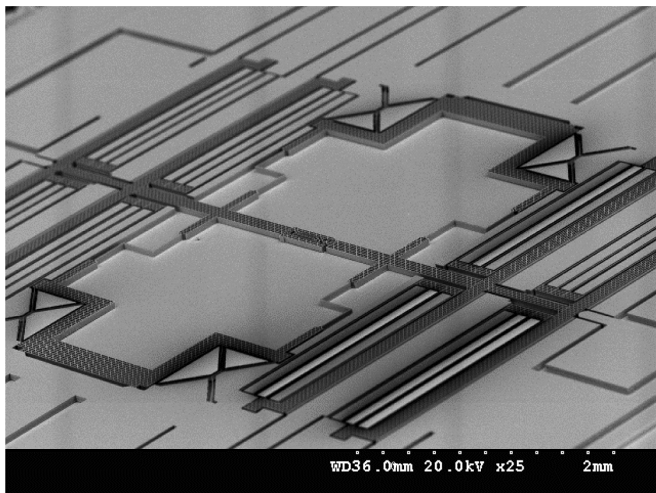


Fig. 11. Large size switching stage obtained with one-step dry etch and release process.

VI. CONCLUSION

On a SOI wafer, when the DRIE process reaches the oxide layer notching may happen depending on the trench aspect ratio and pattern shape. Notching effect is a result of the topography-dependent charging of plasma etching, which causes potential difference deflecting ions that bombard the lower corners of the trenches. Although notching is a harmful effect in many cases, we show here that we can take advantage of it. With proper layout according to simple rules, micro devices are fabricated and released in a single step, or at least, the rules allow a stiction free wet release. The notching creates a wider gap below the structure preventing its failure later during the process and during its use. By removing the stiction problem, this technology has allowed to design complicated micro devices with large size on SOI substrate.

REFERENCES

[1] C. Marxer and N. F. de Rooij, "Micro-Optical-Mechanical 2 × 2 switch for single-mode fibers based on plasma-etched silicon mirrors and electrostatic actuation," *J. Lightw. Technol.*, vol. 17, no. 1, pp. 2–6, Jan. 1999.

[2] H. Toshiyoshi, M. Mita, and H. Fujita, "A MEMS piggyback actuator for hard-disk drives," *J. Microelectromech. Syst.*, vol. 11, no. 6, pp. 648–654, Dec. 2002.

[3] O. Gigan, H. Chen, O. Robert, S. Renard, and F. Marty, "Fabrication and characterization of resonant SOI micromechanical silicon sensors based on DRIE micromachining, freestanding release process and silicon direct bonding," *Proc. SPIE*, vol. 4936, pp. 194–204, 2002.

[4] H. B. Liu and F. Chollet, "Optical switch based on moving polymer waveguides and self-latching structure," *Int. J. Comput. Eng. Sci.*, vol. 4, no. 3, pp. 447–450, Sep. 2003.

[5] C. H. Mastrangelo and C. H. Hsu, "Mechanical stability and adhesion of microstructure under capillary forces—part I: Basic theory," *J. Microelectromech. Syst.*, vol. 2, no. 1, pp. 33–43, Mar. 1993.

[6] M. Madou, *Fundamentals of Microfabrication*. Boca Raton, FL: CRC Press, 1997, pp. 235–236.

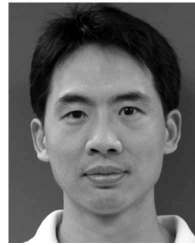
[7] J. Y. Kim and C. J. Kim, "Comparative study of various release methods for polysilicon surface micromachining," in *Proc IEEE 10th Annu. Int. Workshop on Micro Electro Mechanical Systems: An Investigation of Micro Structures, Sensors, Actuators, Machines and Robots (Cat.CH36021)*, 1997, pp. 442–447.

[8] T. Abe, W. C. Messner, and M. L. Reed, "Effective methods to prevent stiction during post-release-etch processing," in *Proc. IEEE Microelectromechanical Systems (MEMS '95)*, Amsterdam, The Netherlands, 1995, pp. 94–99.

[9] G. K. Fedder, J. C. Chang, and R. T. Howe, "Thermal assembly of polysilicon microactuators with narrow-gap electrostatic combdrive," in *Proc. Technical Digest: 1992 Solid State Sensor and Actuator Workshop*, Hilton Head Island, SC, 1992, pp. 63–68.

[10] C. H. Mastrangelo and G. S. Saloca, "A dry-release method based on polymer columns for microstructures fabrication," in *Proc. Microelectromechanical Systems (MEMS '93)*, Ft. Lauderdale, FL, 1993, pp. 77–81.

[11] T. A. Lober and R. T. Howe, "Surface micromachining processes for electrostatic microactuator fabrication," in *Proc. Technical Digest: 1988 Solid State Sensor and Actuator Workshop*, Hilton Head Island, SC, 1988, pp. 59–62.
[12] M. R. Houston, R. Maboudian, and R. T. Howe, "Ammonium fluoride anti-Stiction treatments for polysilicon microstructures," in *Int. Conf. Solid State Sensors and Actuators*, Stockholm, Sweden, 1995, pp. 210–213.
[13] G. T. Mulhern, D. S. Soane, and R. T. Howe, "Supercritical carbon dioxide drying of microstructures," in *Int. Conf. Solid-State Sensors and Actuators*, Yokohama, Japan, 1993, pp. 296–299.
[14] P. T. Docker, P. K. Kinnell, and M. C. L. Ward, "Development of the one-step DRIE dry process for unconstrained fabrication of released MEMS devices," *J. Micromech. Microeng.*, vol. 14, no. 7, pp. 941–944, Jul. 2004.
[15] G. S. Hwang and K. P. Giapis, "On the origin of the notching effect during etching in uniform high density plasmas," *J. Vacuum Sci. Technol. B: Microelect. Process. Phenom.*, vol. 15, no. 1, pp. 70–87, Jan.–Feb. 1997.
[16] M. Chabloz, J. Jiao, Y. Yoshida, T. Matsuura, and K. Tsutsumi, "Method to evade microloading effect in deep reactive ion etching for anodically bonded glass-silicon structures," *Proc. IEEE Microelectromechanical Systems (MEMS)*, pp. 283–287, 2000.
[17] K. P. Giapis and G. S. Hwang, "Pattern-dependent charging and the role of electron tunneling," *Jpn. J. Appl. Phys. Part 1: Regular Papers, Short Notes, Review Papers*, vol. 37, no. 4B, pp. 2281–2290, Apr. 1998.
[18] F. Lärmer and A. Schilp, "Method of anisotropically etching silicon," U.S. Patent Specification 5501893, German Patent Specification DE4 241 045.
[19] A. A. Ayon, X. Zhang, and R. Khanna, "Ultra deep anisotropic silicon trenches using deep reactive ion etching (DRIE)," in *Proc. Solid-State Sensor and Actuator Workshop*, Hilton Head Island, S.C, 2000, pp. 339–342.
[20] P. T. Docker, P. Kinnell, and M. C. L. Ward, "A dry single-step process for the manufacture of released MEMS structures," *J. Micromech. Microeng.*, vol. 13, no. 5, pp. 790–794, Sep. 2003.
[21] B. E. Volland, "Profile simulations of gas chopping etching process," Ph.D. dissertation, Institute of Physics, University of Kassel, Kassel, Germany, 2004.



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