High performance InP-based heterostructure barrier varactors in single and stack configuration

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Single (SHBV) and dual (DHBV) heterostructure barrier varactors with $AlAs/In_{0.52}Al_{0.48}As$ blocking conduction layers have been fabricated and characterised. The devices, whose electrical properties scale with layer complexity, exhibit, for a DHBV scheme, leakage currents as low as $10 A/cm^2$ at 12V, a zero bias capacitance of $1 fF/\mu m^2$, and a capacitance ratio of 5:1.

Introduction: A single barrier varactor, also known as heterostructure barrier varactor (HBV), first proposed in 1989 [1], consists of a large bandgap semiconductor sandwiched between two *n*-type smaller bandgap cladding layers. The potential barrier, thus formed in the conduction band, prevents conduction through the structure, so that each cladding layer can be depleted according to bias conditions. For symmetric structures about the centre of the barrier, the devices exhibit a symmetric nonlinear capacitance relationship about zero bias. This property suppresses the generation of even harmonics when a pump signal is applied to the sample so that these devices are good candidates for high efficiency millimetre and submillimetre wave multipliers. Besides, by epitaxially stacking several barriers in series [2], further advantages are expected: in particular an increase in the power handling capabilities. So far however, most of the fabricated devices suffered from high leakage current resulting mainly from the poor blocking of barriers. In this letter, we show how this shortcoming can be alleviated using a stair-like AlInAs/AlAs blocking barrier which was used for fabricating single heterostructure barrier varactor (SHBV) and dual heterostructure barrier varactor (DHBV) diodes.

Layer	Thickness
InGaAs 5×10^{18} cm^{-3}	500nm
InGaAs 1×10^{17} cm^{-3}	300
InGaAs undoped	5
InAlAs undoped	5
AlAs undoped	3
InAlAs undoped	5
InGaAs undoped	5
InGaAs 1×10^{17} cm^{-3}	300
InGaAs 5×10^{18} cm^{-3}	500
InP substrate	

(x2 for DHBVs: layers from InGaAs undoped to InGaAs 1×10^{17} cm^{-3} 300)

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Fig. 1 *Growth parameters for single heterostructure barrier varactor (SHBV) and dual heterostructure barrier varactor (DHBV)*

Growth and processing: Fig. 1 depicts the growth sequence of fabricated devices. One way to prevent any leakage current over (thermionic emission) and through (tunnelling) the barrier, is to make use of pseudomorphic $AlAs/In_{0.53}Ga_{0.47}As$ epilayers grown on an InP substrate. Such a material system was previously used for successfully fabricating high breakdown voltage quantum barrier varactor diodes [3], and more recently high current resonant tunnelling diodes [4]. The key advantage afforded by this material system is the very high conduction band offset between AlAs and $In_{0.53}Ga_{0.47}As$ of ~1.2eV at Γ conduction band minima. However, the growth of thick AlAs layers may be unfavourable owing to the high lattice mismatch between AlAs and $In_{0.53}Ga_{0.47}As$, and the occurrence of parasitic conduction through the X valley. On this basis, we preferred to sandwich an AlAs layer with a moderate thickness between two $In_{0.48}Al_{0.52}As$ layers. Starting from a semi-insulating Fe-doped InP substrate, all the epilayers were grown in a gas source molecular beam epitaxy Riber machine. In practice, alloy composition and growth rates were deduced from RHEED intensity oscillation measurements of InP (on InP) and of GaAs and AlAs (on GaAs). Silicon doping levels were estimated from Hall measurements of calibration structures. The growth was performed without interruption at ~520°C for both binary and ternary compounds.

The test structure consists of a mesa diode with top and side ohmic contacts with overlay gold films for wafer probing the samples without requiring access of coplanar waveguides [4]. It was fabricated using three photolithography masks. $H_3PO_4/H_2O_2/H_2O$ solution was used for mesa etching and sequential Ni/Ge/Au/Ti/Au metallisations were used for the ohmic contacts. Several sizes of diode, with diameters ranging from 10 to 40μm, have been fabricated, along with a TLM pattern for measuring the contact resistance after RTA.

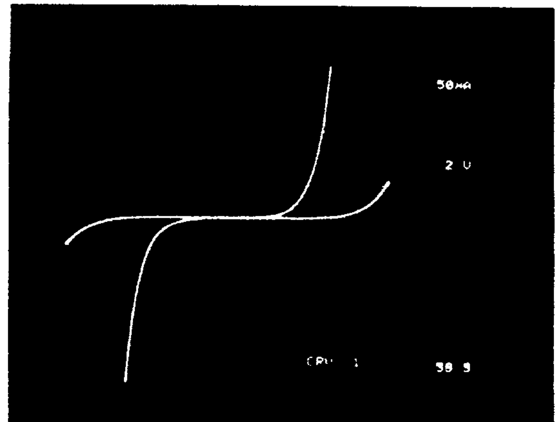

Fig. 2 *Comparison of current voltage characteristics for SHBV and DHBV samples measured at room temperature*

Results: Fig. 2 shows the current voltage characteristics for SHBV and DHBV respectively, measured at room temperature. The mesa diameter is 40μm. For both samples, excellent symmetry can be noted between the two bias directions. This high degree of symmetry is quite remarkable and attests to the high quality of the epilayers, notably to a good morphology of direct and inverse heterointerfaces. It can be seen that the barrier plays its role entirely by maintaining a low level of conduction below 6V ($J < 10 A/cm^2$) for a typical SHBV and twice this value for a DHBV, in agreement with the assumption that the total voltage should be twice as high. Calculations of the I(V) characteristics achieved by solving Schrödinger and Poisson's equations, the results of which will be reported elsewhere, also show a good fit between measured and calculated data. On the basis of this agreement, it is believed that the conduction mechanisms are relatively pure in the sense that the calculations permit the determination of the correct quantum transmission probabilities through and over the barrier, without involving a defect-assisted contribution. However, an ambiguity about the mechanism responsible for conduction still subsists close to the breakdown voltage. In Kollberg's original paper [1] avalanche mechanism was evoked as a possible limiting factor. For the devices under test and made from low gap material, it seems that impact ionisation in the depleted $In_{0.53}Ga_{0.47}As$ can contribute to the increase of current at voltage exceeding 6V. A rough estimate of the breakdown voltage V_b can be made from the work of Sze and Gibbons for abrupt *p-n* junctions ([5], eqn. 5(*a*)). We calculated $V_b = 6.3V$, which is quite comparable to the experimental breakdown voltage. This estimate has to be supported by systematic temperature measurements in order to discriminate between tunnelling and avalanche mechanisms. Nevertheless, if the latter process becomes dominant, this means that it could be useless to further increase the barrier thickness in order to increase the power handling of a basic structure.

With reference to the the capacitance measurements, Fig. 3 compares the capacitance-voltage characteristics of SHBV and DHBVs measured at 500MHz. Here again, the capacitance level closely scales with layer complexity with a factor of two between single and dual structures. Also important is the fact that we

recovered the same impedance level for an area two times larger, with the associated benefit of a power handling which scales in that case as the square of the number of stacked varactor structures. The ratio between the capacitance at equilibrium C_0 (2fF/μm^2 for SHBV) and the capacitance at saturation C_s, practically obtained under punch through conditions ($C_s \sim \varepsilon/l$, with l = 300nm), is ~5:1 which is comparable to the best values published in the literature [3 – 6].

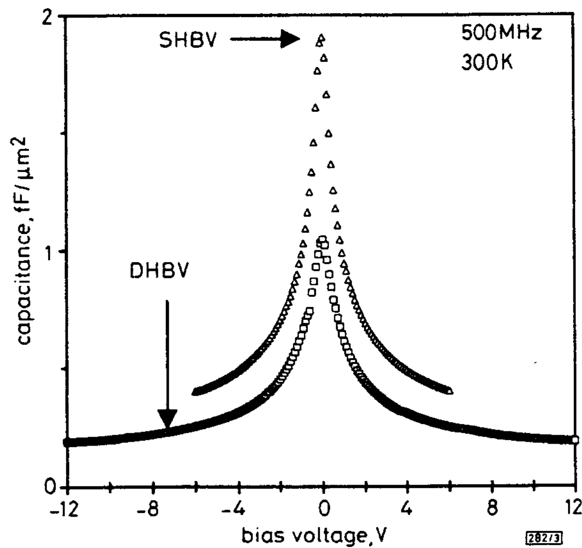

Fig. 3 *Comparison of capacitance-voltage characteristics measured at 500 MHz*

From these capacitance measurements, we can estimate the cutoff frequency $F_c = (S_{max}-S_{min})/2\pi R_s$ where R_s is the series resistance and S the elastance ($S = 1/C$). An order of magnitude of the series resistance can be predicted from contact resistance measurements and resistance data of the mesa material. Using the TLM pattern available on the mask we measured $R_c = 2 \times 10^{-7} \Omega.cm^2$, which was found to be of the same order of magnitude to the epilayer resistance. Using these data, a cutoff frequency of ~6THz can be predicted for a basic varactor structure.

Conclusion: High performance heterostructure barrier varactors making use of the blocking properties of a stair-like InAlAs/AlAs potential barrier, have been successfully fabricated with predicted cutoff frequency as high as 6THz. By epitaxially stacking two barriers in series, it was also demonstrated that the electrical properties perfectly scale with the number of varactor structures, and that the devices can handle 12V without significant leakage current.

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